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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,217	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 November 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 have been presented for examination. Claims 1-20 have been rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-6 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3. Claim 1 recites a virtual microcontroller having *means for* detecting a sequence of instructions, for computing a conditional jump address, and for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution. The disclosure does not adequately describe what is meant by these limitations. For example, the disclosure (page 27, line 5, through page 28, line 8) describes these steps in narrative, often personifying the virtual microcontroller ("the virtual microcontroller *always assumes* that a jump condition is true and computes the target jump as if the condition requiring the jump is satisfied," page 27, lines 5-7). The fact that this regards a "virtual microcontroller", the tangible embodiment of which is open to interpretation, further clouds what is meant by a virtual microcontroller that *assumes*. Is this performed by hardware? Software? Is this an execution model? A programming technique? A particular set of programming instructions? Specialized functions of the instruction set architecture? Additionally, is this assumption based on interpreting assembly instructions, as exemplified by the disclosure (page 26, lines 17-29), or by examining machine code as executed? The other limitations are vaguely described and it is impossible to determine precisely what is meant by the "means for" limitations of claim 1.

4. Claims 1-20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. The limitations related to "detecting a sequence of instructions", present in all independent claims 1, 6, and 14, are inadequately described in the disclosure. The disclosure provides an example of the instructions that are to be detected (page 26, lines 17-29), however nowhere considers how these instructions are to actually be detected in the general case. The breadth of the instructions described by independent claims 1, 6, and 14 includes very nearly any program which includes at least one I/O read instruction and a conditional jump. The disclosure in no way describes the type of detection performed on the innumerable instruction sequence scenarios encompassed by the extremely broad recited limitations.

6. Claims 1-20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Independent claims 1, 6, and 14 are not enabled by the disclosure where they refer to steps such as "detecting a sequence of instructions". The disclosure provides

inadequate written description of the process of "detection", and these claims define the "sequence of instructions" so vaguely that they encompass basically any non-trivial set of computer program instructions. Under these circumstances, a person of ordinary skill in the art could not have any reasonable expectations of building and using the claimed invention, as it is essentially unclear what the claimed invention attempts to accomplish.

7. MPEP 2164.01(a) provides at least eight factors to consider when determining whether there is sufficient enablement.

(A) The breadth of the claims;
(B) The nature of the invention;
(C) The state of the prior art;
(D) The level of one of ordinary skill;
(E) The level of predictability in the art;
(F) The amount of direction provided by the inventor;
(G) The existence of working examples; and
(H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure.

Regarding these factors, the Examiner remarks:

(A) The independent claims 1, 6, and 14 are so broad that they reasonable cover any non-trivial set of computer instructions, yet require detecting a particular sequence of vaguely defined instructions and are therefore extremely broad.

(B) The field of in-circuit emulation is widely regarded as extremely complicated and the union of numerous sciences, such as signals, electronic circuit design, computer engineering, and the like.

(C) The prior art in the area of in-circuit emulation is hardly concerned with performing analyses of compiled or interpreted computer program source code;

the combination of such methods may be novel or non-obvious but therefore it is even more essential that the inventor provide adequate disclosure.

(E) Countless inventions have been offered that attempt to reduce the development time for integrated circuits that is lost due to poor design, unforeseen complications of the design, and generally the inability to accurately predict the results of the design process. Indeed, Applicants' invention attempts to enhance the reliability of an in-circuit emulation.

(F) As set forth above, the steps of detecting a particular sequence of vaguely defined instructions is inadequately described by the disclosure. The passages of the disclosure related to this detection are narrative and devoid of any details of implementation.

(G) The Examiner would be pleased to have evidence of working examples. Applicant has not provided any disclosure of working examples, and the absence of an Information Disclosure Statement filed under 37 CFR 1.97 and 1.98 is noted.

(H) Due to the lack of direction provided by the disclosure, a person attempting to make and use the claimed invention would be left to his own devices to accomplish the entire process of discovery or invention pertaining to detecting the vaguely defined sequence of instructions as claimed.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. As a result of the rejections of claims 1-6 under 35 U.S.C. § 112, first paragraph above regarding the "means for" language, it is impossible to determine the metes and bounds of claims 1-6.

10. Regarding claims 1-20, it is unknown what is meant by "detecting a sequence of instructions". For example, it is unknown whether this is performed before, during, or after the execution of the instructions of interest. If the detection is performed before the instructions are executed, it is unclear how or by what capabilities the instructions are detected, since the execution capabilities of the virtual microcontroller are presumably occupied with normal execution. If the detection is performed during or after the instructions are executed, the remaining limitations appear to be inconsequential or irrelevant.

11. It is unclear if these instructions comprise assembly code, as exemplified by the disclosure (page 26, lines 17-29), executable machine code, or some other form.

12. Further, the breadth of "an I/O read instruction followed by a conditional jump instruction" is indeed so broad that it is indeed indefinite. Any sequence of instructions that performs an I/O read instruction and, at some unrelated point in the unforeseeable

future, executes an unrelated conditional jump is covered by this language. For example, the limitations of claim 6 seek patent protection for executing a conditional jump instruction where an I/O read instruction has been executed in the past and some I/O read data will be received at some unspecified future time, such execution occurring in the context of the apparatus recited in the preamble. There is no recited connection between the I/O read, the data received from the I/O read, and the conditional jump instruction. There is no recited connection between the I/O read instruction and the data received from the I/O read, such as reciting that the "I/O read data" is the direct result of the previously recited "I/O read instruction" rather than the direct result of some other I/O read instruction.

In general, the claims are replete with difficulties under at least 35 U.S.C. § 112, first, second, and sixth paragraphs. Because so many of the dependent claims are directly related to the inadequacy of the disclosure under 35 U.S.C. § 112, first paragraph, the Examiner does not feel it would be productive to rely upon speculative interpretations of substantial portions of the disclosure in order to thoroughly treat those claims on the merits. Applicant is respectfully advised to regard the rejections under 35 U.S.C. § 112 set forth above as exemplary and respectfully requested to review the disclosure and claims, in their entirety, for compliance with 35 U.S.C. § 112.

Claim Interpretation

In the interest of compact prosecution, examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984). However, the state of the disclosure and claims in the instant application preclude a limitation-by-limitation assessment of the claimed invention compared to the prior art. Therefore prior art is applied under 35 U.S.C. §§ 102 and 103 in an attempt to expedite prosecution in anticipation of future amendments rather than strictly based upon the Examiner's assumptions. See *In re Steele*, 305 F.2d 859,134 USPQ 292 (CCPA 1962).

Applicants' invention is regarded as:

An in-circuit emulation system (and method employing the system) having a microcontroller coupled to and operating in lock-step with a virtual microcontroller that supports conditional jumps directly related to input / output (I/O) read instructions. In one embodiment, the virtual microcontroller is implemented in a field programmable gate array (FPGA).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,911,059 to Profit, Jr. (Profit) in view of US Patent No. 6,173,419 to Barnett (Barnett).

Profit teaches an in-circuit emulation system (Fig. 7) with numerous features relevant to Applicants' claimed invention:

A processor emulator 202 is typically a commercially available microprocessor-based device (column 6, lines 5-24).

The processor emulator 202 includes a processor 204 coupled to a memory 206 (column 6, lines 11-12). (Official notice is taken that the term *microprocessor* refers to a single unit usually comprising central processing unit, memory, I/O ports.)

The hardware simulator 210 includes a processor model shell 212 which converts a sequence of processor functions to activity at simulated pins of the target processor (column 6, lines 29-32).

For example, assume that the target program 22 (executing on the processor emulator) *contains a memory read instruction* (an I/O read instruction) *that references an address location allocated to the address space of the target circuitry. In this case, a sequence of processor functions is input to the processor model shell 212* (at this point, processor model shell 212 is a virtual equivalent of the processor emulator) *which cause the processor model shell to change the address, data, and control lines at the simulated*

pins to simulate the memory read instruction in the hardware simulator 210 (column 6, lines 35-48).

The hardware simulator 210 and processor model shell 212 typically run on a host computer 214, such as a SUN, HP, or other suitable workstation. [...] *As known by those skilled in the art, the host computer 214 typically contains other software tools to facilitate user interface to the system and the development of the software program which simulates the target circuitry.* [...] *Software debugging tools are likewise typically contained on the host computer 214* (column 6, lines 49-60).

Communications between the processor emulator 202 and the hardware simulator 210 is handled by a communications interface 220 (functionally equivalent to a "pod") (column 7, lines 14-30).

The second function performed by the communications interface 220 is a resynchronization of the target program 22 and target circuitry (the emulator microcontroller and virtual microcontroller operate synchronously) (column 7, lines 49-54).

Setting the time interval to zero would cause synchronization to occur at the execution of each instruction (the emulator microcontroller and virtual microcontroller operate in lock-step) (column 11, lines 40-43, regarding the configuration described primarily at column 10, lines 32-58).

Profit teaches a method of execution wherein the virtual microcontroller and emulated microcontroller remain synchronized despite the latency inherent in I/O operations (primarily column 11, line 44 – column 12, line 35).

While Profit teaches that the hardware simulator (including the processor model shell, functionally equivalent to a virtual microprocessor) is "typically implemented" on a host computer, such as a SUN, HP, or other suitable workstation, Profit does not explicitly teach that the hardware simulator be implemented in an FPGA.

Barnett teaches the use of an FPGA as a hardware emulator (abstract; column 2, lines 11-16; column 5, lines 38-56). Barnett teaches that the advantage of such an arrangement is the reuse of the hardware emulator for different configurations (column 2, lines 41-51).

It would have been obvious for a person of ordinary skill in the art at the time of Applicants' invention to implement the hardware simulator taught by Profit in an FPGA, according to the method taught by Barnett, in order to provide an in-circuit emulator system that facilitates emulating the emulated microcontroller in different configurations of target circuitry. The advantages of such an arrangement would be obvious to a person of ordinary skill in the art, as it would increase the testing capabilities and reduce the costs and time associated with testing. The combination could be achieved by implementing the hardware simulator taught by Profit on an FPGA connected to and configured by the host computer, wherein the emulation process taught by Profit proceeds as taught except where interaction with the hardware simulator would necessarily be interaction with the configured FPGA.

Any limitations not specifically addressed would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention in light of his own knowledge of the particular art as well as the Profit and Barnett references, subsequently they are not granted patentable weight.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to

the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
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